DDR Penetrates Mobile Computing

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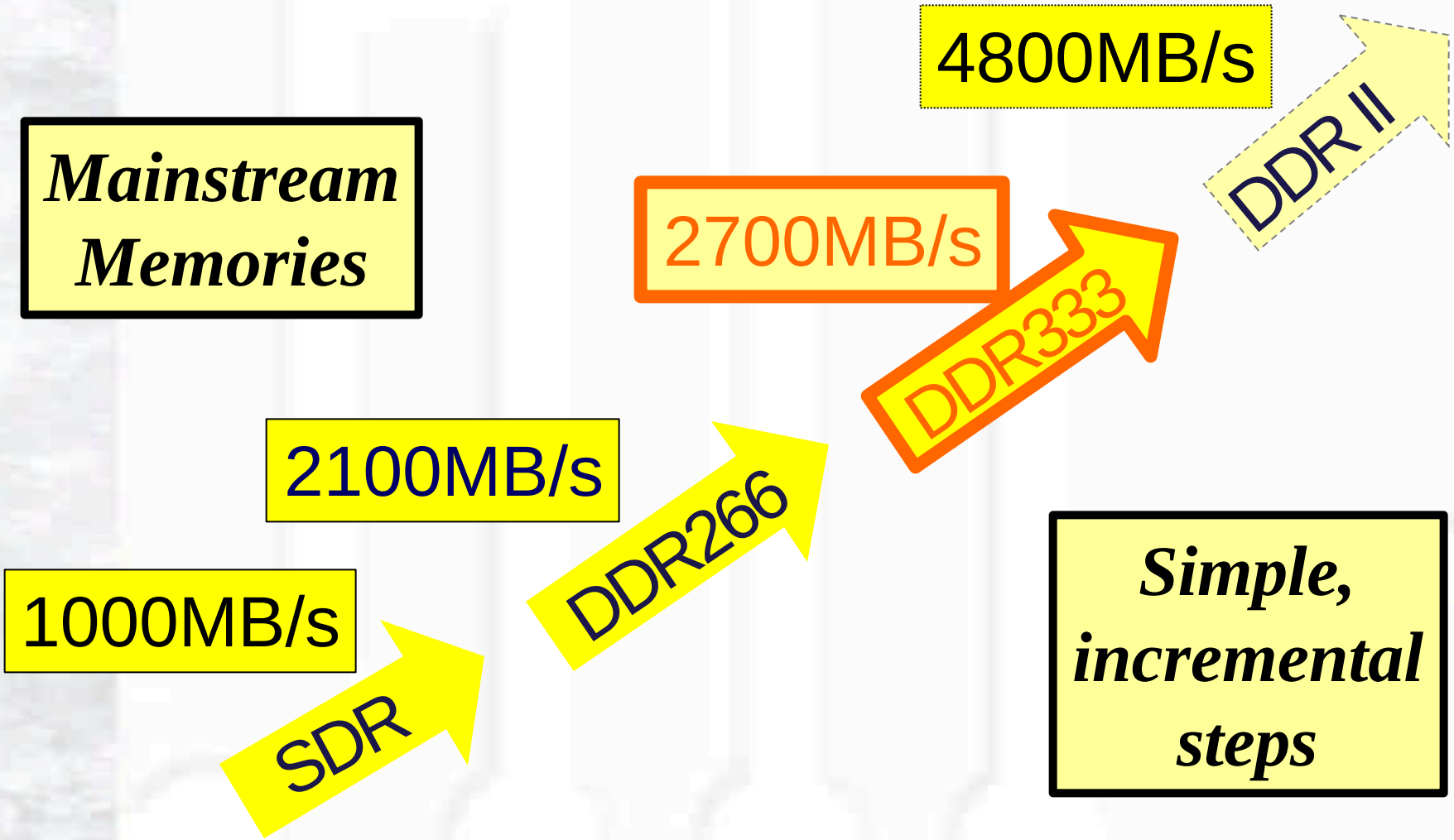
Agenda

- Why DDR for Mobile?
- Standard versus cached DRAMs
- DDR Configurations
- Introducing the DDR MicroDIMM
- Mobile System Design Guidelines

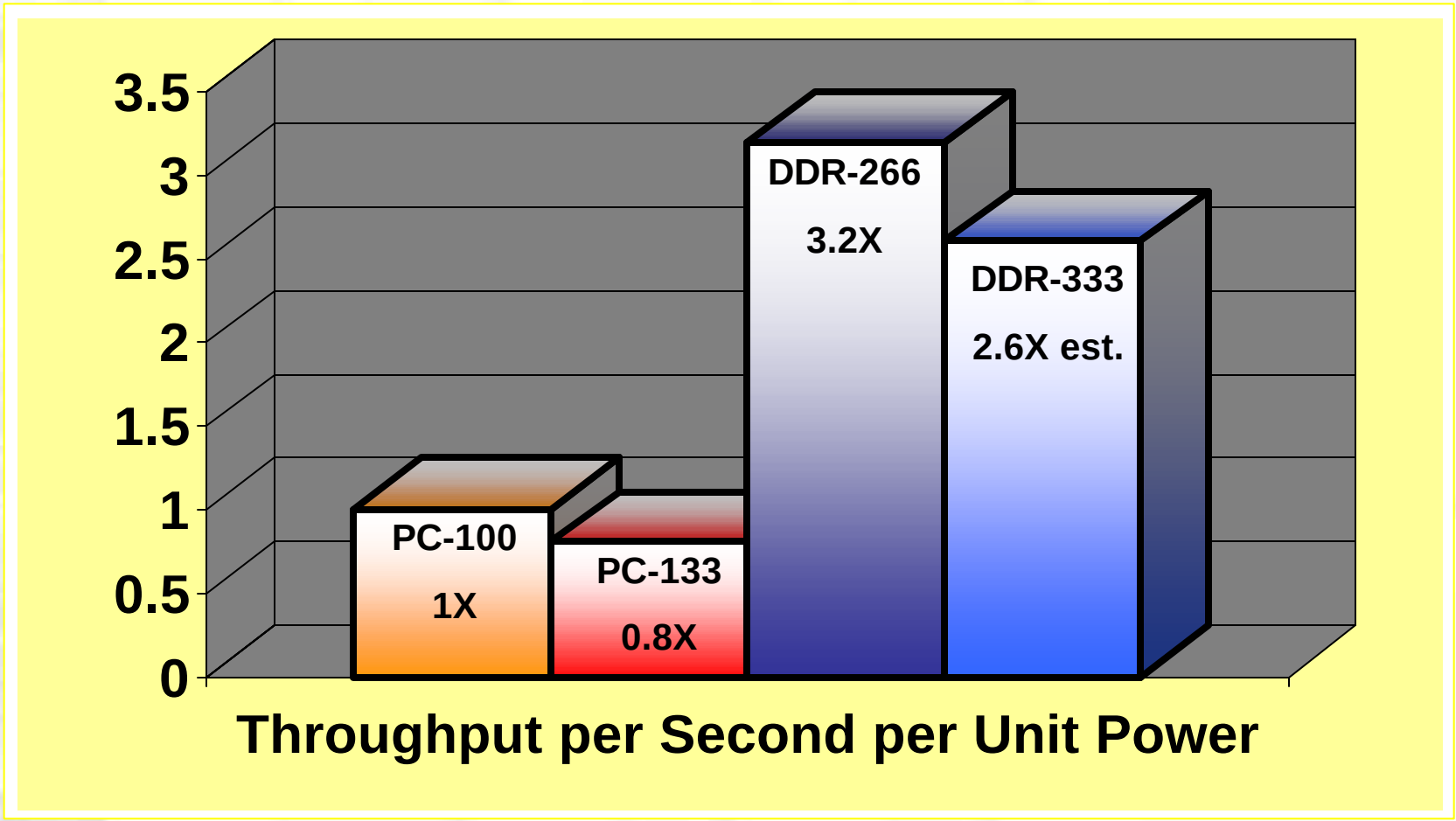
Reasons for DDR in Mobile

- Performance
- Power
- Form factors

SDRAM Evolution



Power: DDR vs SDR



DDR Power Management

Power State*	Relative Power	Clocks of Latency
Active on	100%	0
Inactive on	12%	3
Active off	4%	1
Inactive off	0.2%	4
Sleep	0.4%	200

Open Page

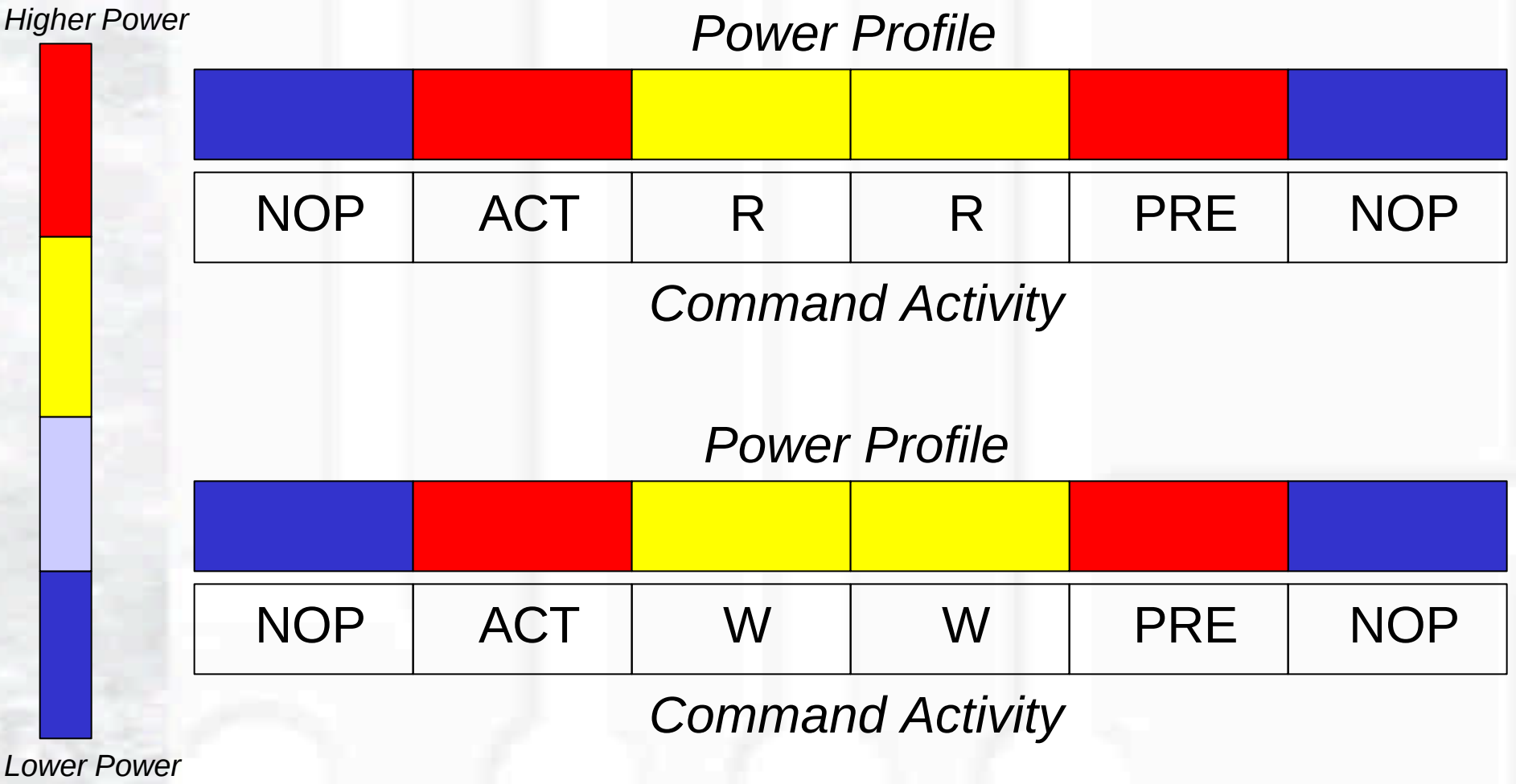
Closed Page

* Not industry standard terms – simplified for brevity

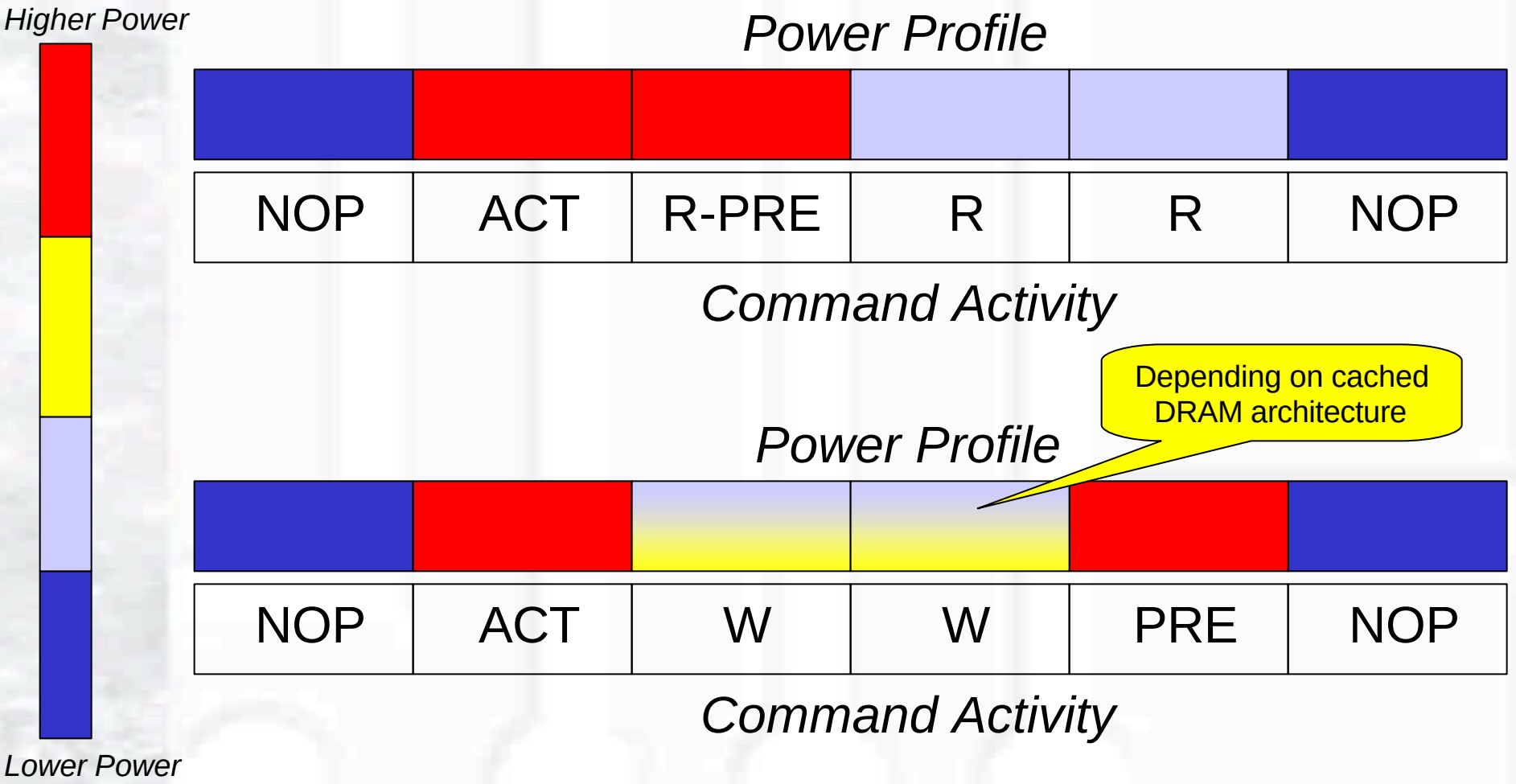
Implications: Mobile Power

- Encourages closed page policy
  - Precharge banks as soon as data read
  - Takes latency hit to reactivate

Closed Page Power Profile



Cached DRAM Power Profile



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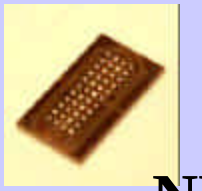
Standard vs Cached

- Cached DRAM architectures save power
  - Improved closed page performance
  - Latency reduction on page hits
  - Lower power profile

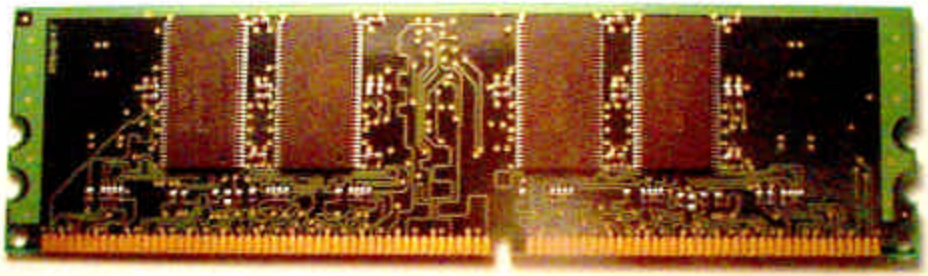
(See my other presentation at Platform 2001… "An Analysis of Virtual Channel and Enhanced Memories Technologies")

DDR Configurations

TSOP-II

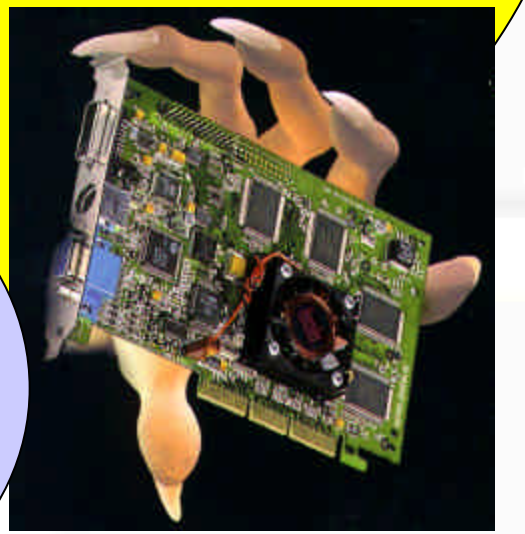


NEW!
FBGA

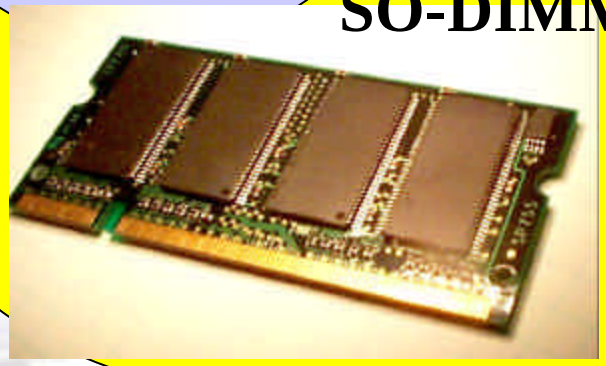


DIMM

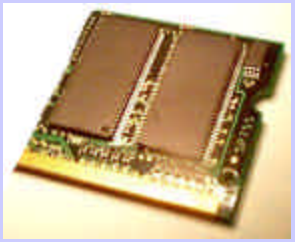
TQFP



SO-DIMM



NEW!
MicroDIMM



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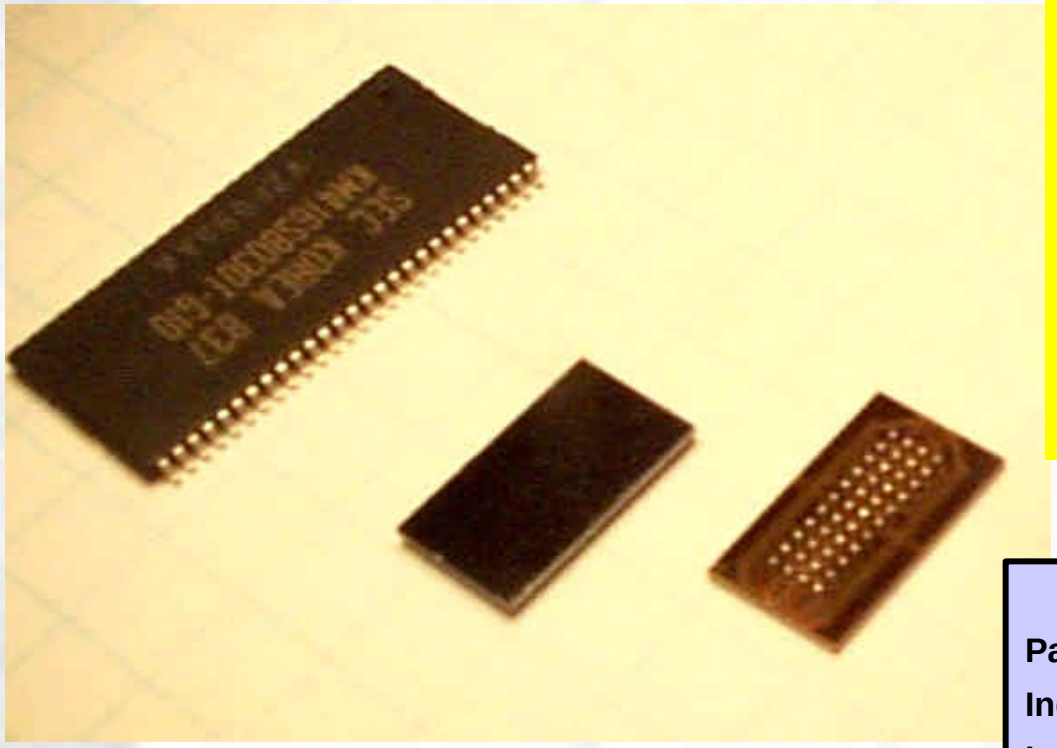
Next: Small Packages



FBGA (fine pitch BGA)

- Lower inductance
- Lower capacitance
- Smaller footprint
- Tighter layouts enabled

Details:

Package size = 104 mm^2 = 54% smaller

Inductance: 1.7nH lower

Inductance variation, pin to pin: 3X less

Capacitance: 0.5pF lower

Performance gain: 300ps of data valid time

DDR Chip Configurations

- **TQFP** devices for point to point
  - x32 … 64Mb, 128Mb coming
  - 100 pins, 16 x 22 mm footprint
- **TSOP** devices
  - x4, x8, x16 … 64Mb, 128Mb, 256Mb
  - 66 pins, 12 x 22 mm footprint
- **FBGA** selection in process
  - x4, x8, x16 … 128Mb, 256Mb, 512Mb/1Gb coming
  - 60 ball, 6.4 x 11 mm minimum footprint

DDR Module Configurations

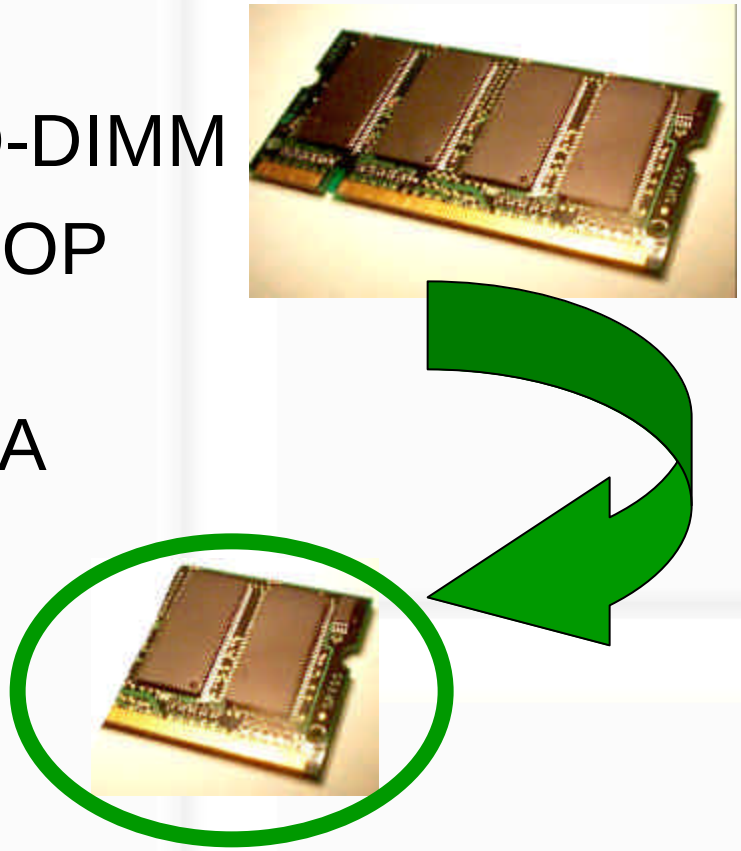
- **DDR SO-DIMM** – done!
  - Sockets, modules in production
- **DDR MicroDIMM** – in process
  - Task group active
- System application combinations
  - One module only
  - Soldered down + module
  - Two modules

Next: DDR MicroDIMM

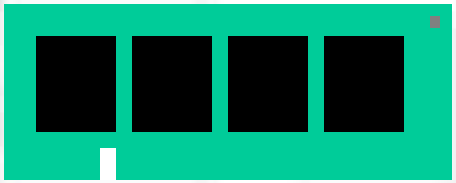
- Half the size of the DDR SO-DIMM
- Half the capacity if using TSOP

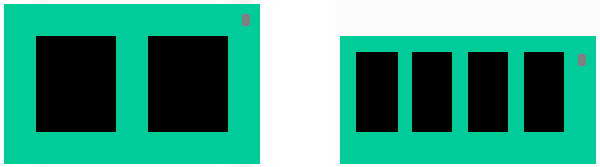
  – or –

- Same capacity if using FBGA
- Target markets:
  - PDAs
  - Internet appliances
  - Subnotebook computers



SO- and Micro- DIMMs





DDR SO-DIMM

TSOP:
67.6 x 31.75 mm = 2146 mm^2

4 or 8 devices

200 pins on 0.6 mm pin pitch (supports ECC)

FBGA:
Under consideration if needed

DDR MicroDIMM

TSOP:
45.5 x 30 mm = 1365 mm^2

4 devices

172 pins on 0.5 mm pin pitch (no ECC)

FBGA:
45.5 x 25 mm = 1137 mm^2

4 or 8 devices

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Module Status

- DDR SO-DIMM
  - DDR266 validated
  - DDR333 under analysis
  - Looking okay to 333 MHz with TSOP
- DDR MicroDIMM
  - TSOP easy, DDR266/333 speeds
  - FBGA package needed to fit 8 chips
  - Possible schedule
    - Sample April 2001
    - Approved spec June 2001

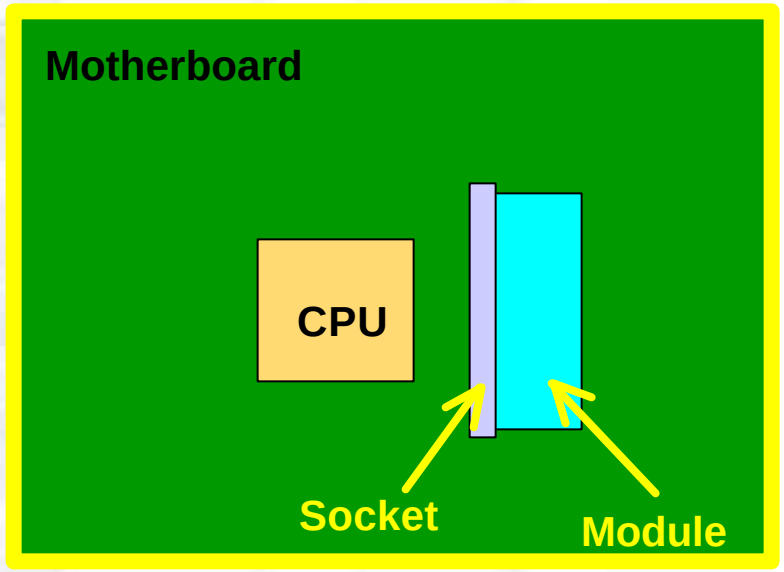
Module Densities

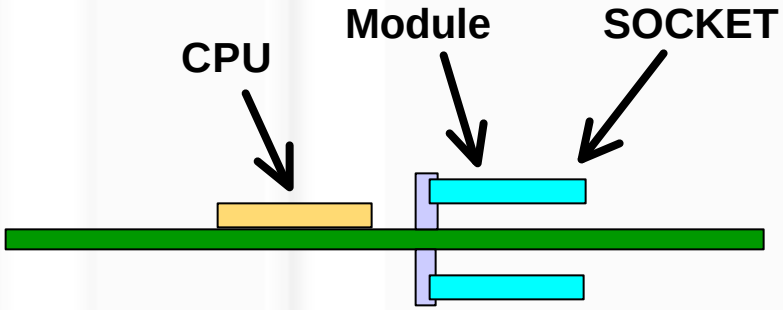
	SO-DIMM				MicroDIMM		
Raw Card	64 (Mb)	128 (Mb)	256 (Mb)	Raw Card	64 (Mb)	128 (Mb)	256 (Mb)
A: 8 TSOPs (MB)	64	128	256	A: 4 TSOPs (MB)	32	64	128
B: 8 TSOPs (MB)	64	128	256	B: 4 FBGAs (MB)	32	64	128
C: 4-5 TSOPs (MB)	32	64	128	C: 8 FBGAs (MB)	64	128	256

Small System Configurations

- One data bus, one address bus
- Point to point, single socket
  - Series damped data, address, clock
- Two sockets
  - SSTL_2 terminated data
  - Series damped address, clock
  - Top/bottom or butterfly arrangement

Top/Bottom Mobile Modules

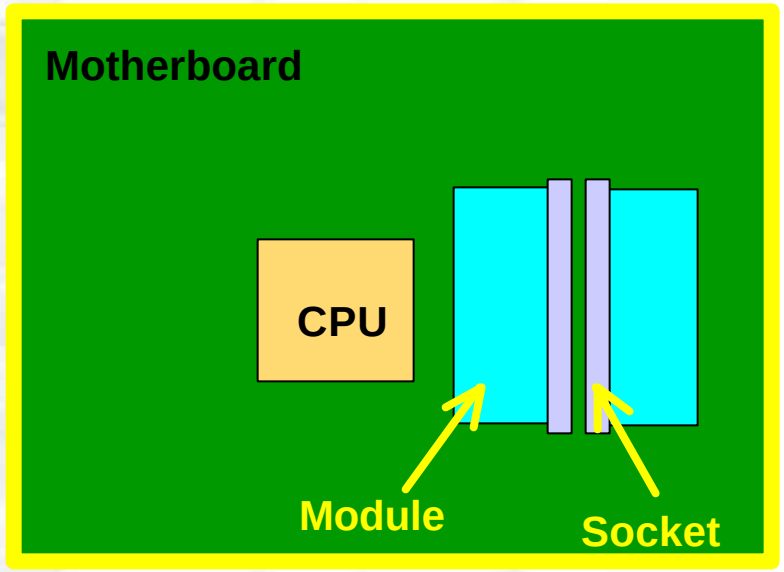


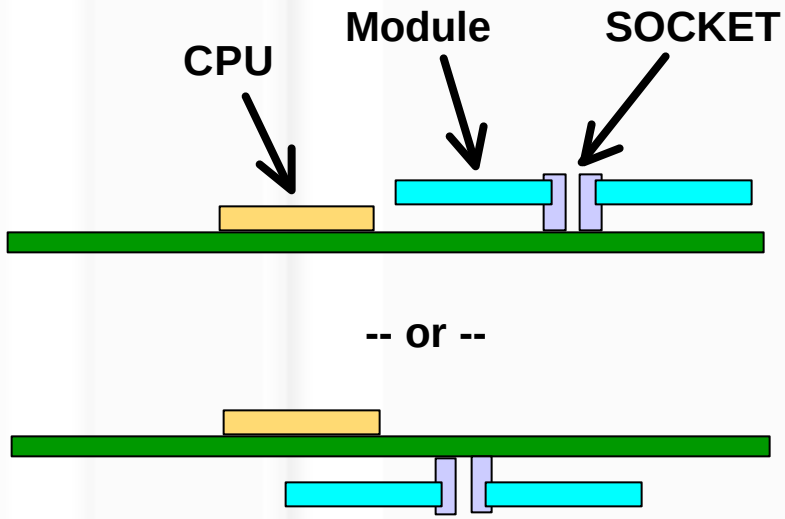


- Standard for many current full size notebooks
- Hard to get at one of the modules
- Thickest form factor

Note: There may be patents regarding use of these layouts

Butterfly Mobile Modules





- Perfect for thin/light notebooks & subnotes
- Single access door to both modules
- Also good for small form factor desktop PCs

Note: There may be patents regarding use of these layouts

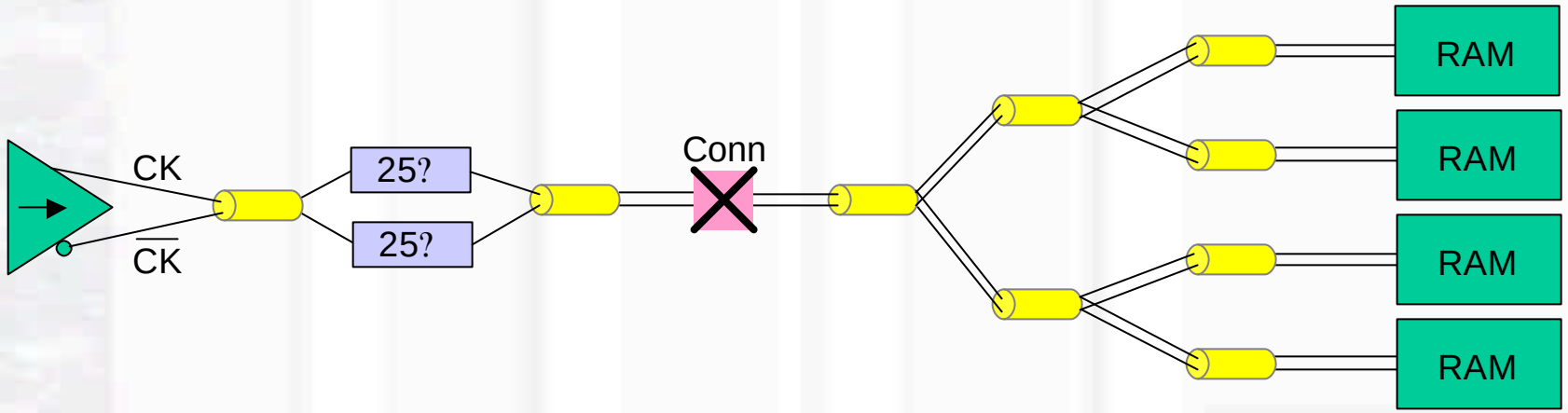
MicroDIMM Designs

You know the DDR SO-DIMM, so…

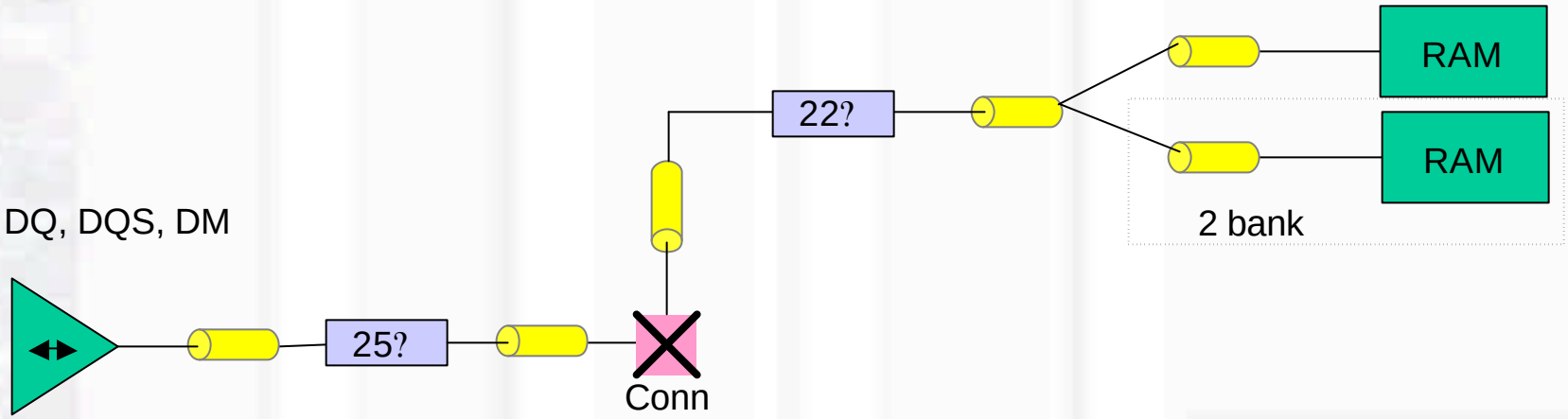
…let's focus on the MicroDIMM design

First, system configurations…

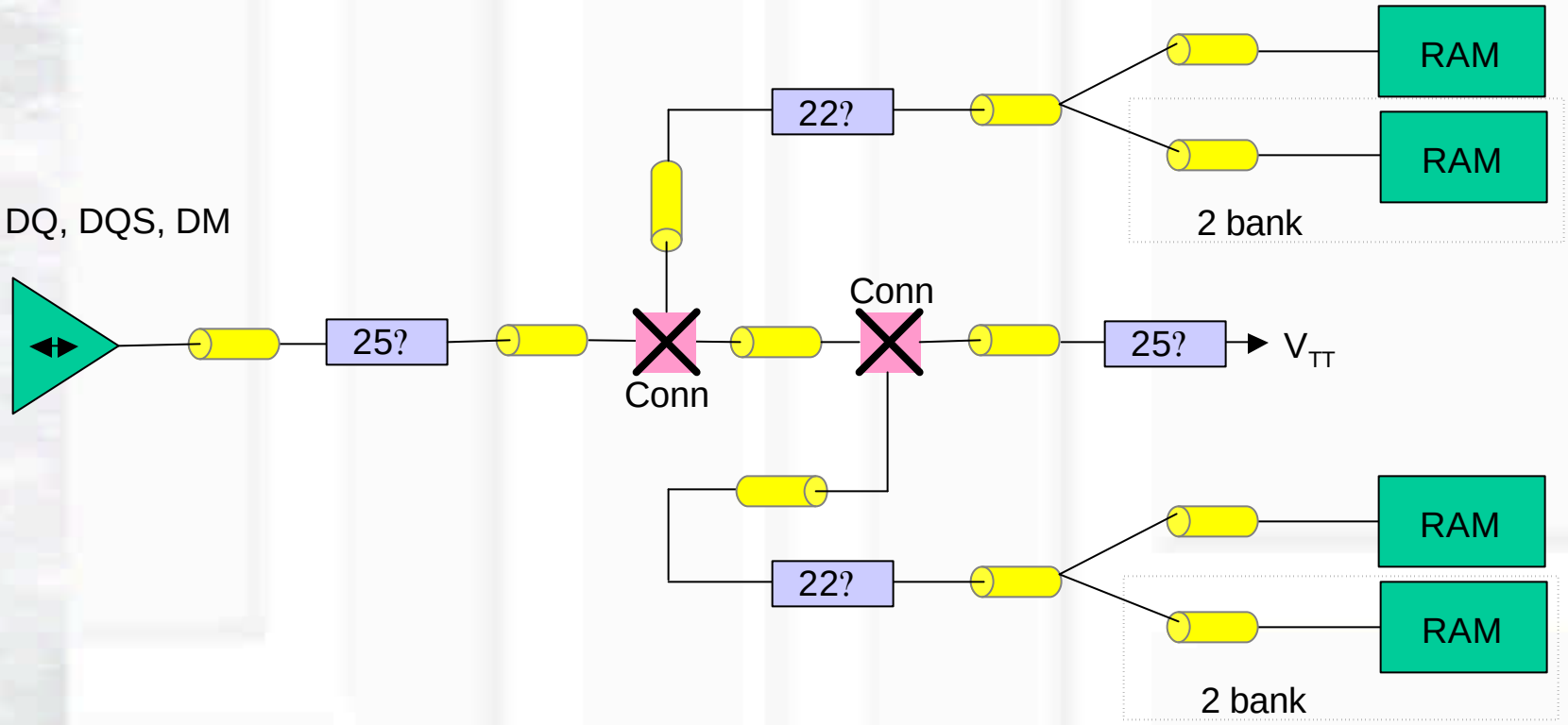
Clock Topology



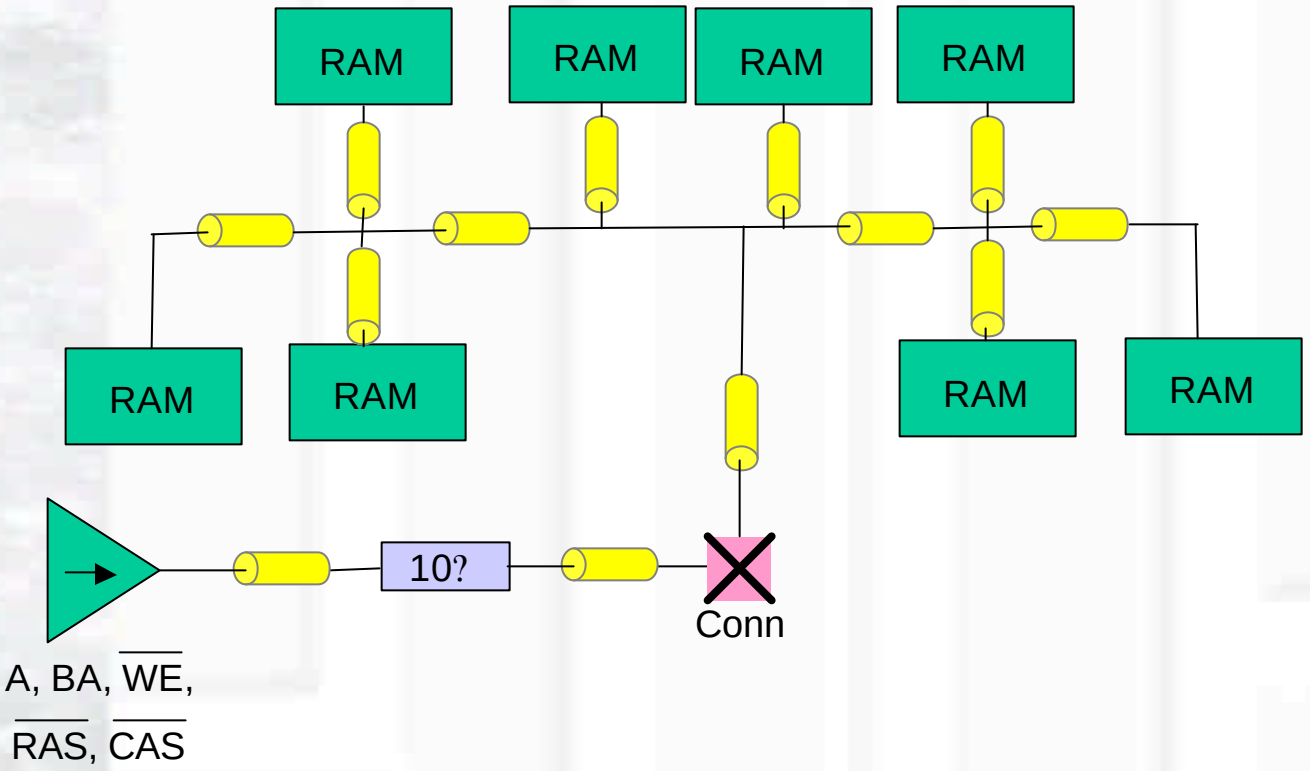
Data Topology, 1 Slot



Data Topology, 2 Slot

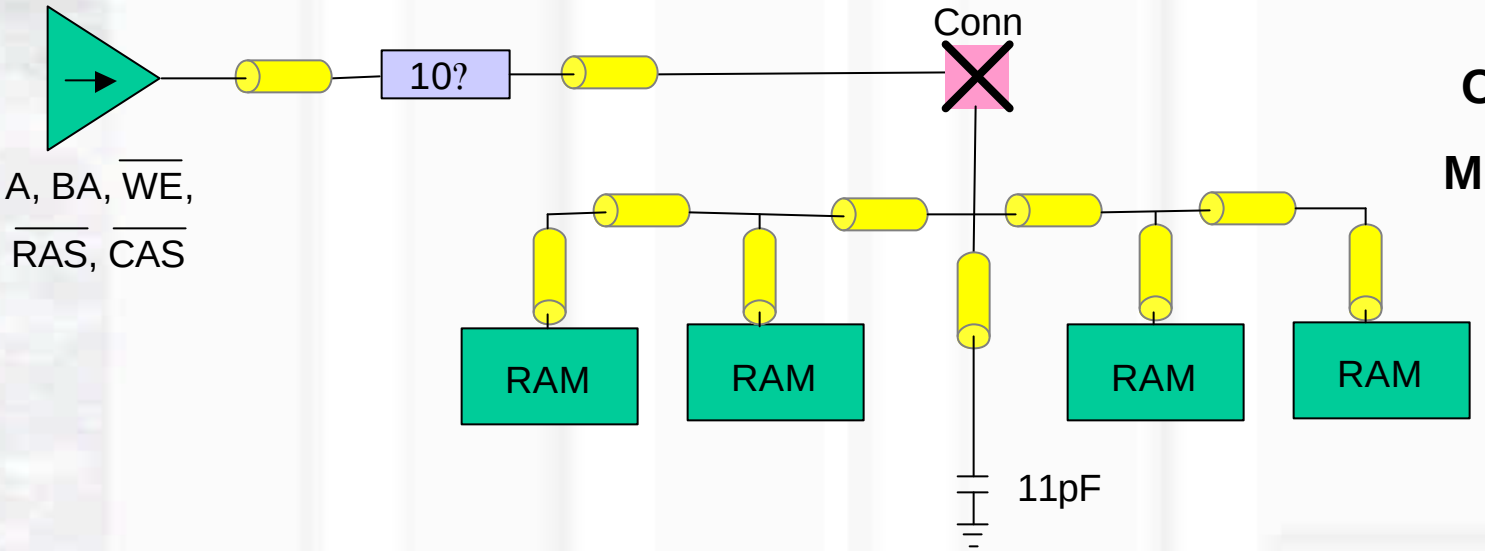


A/C Topology, 1 Slot



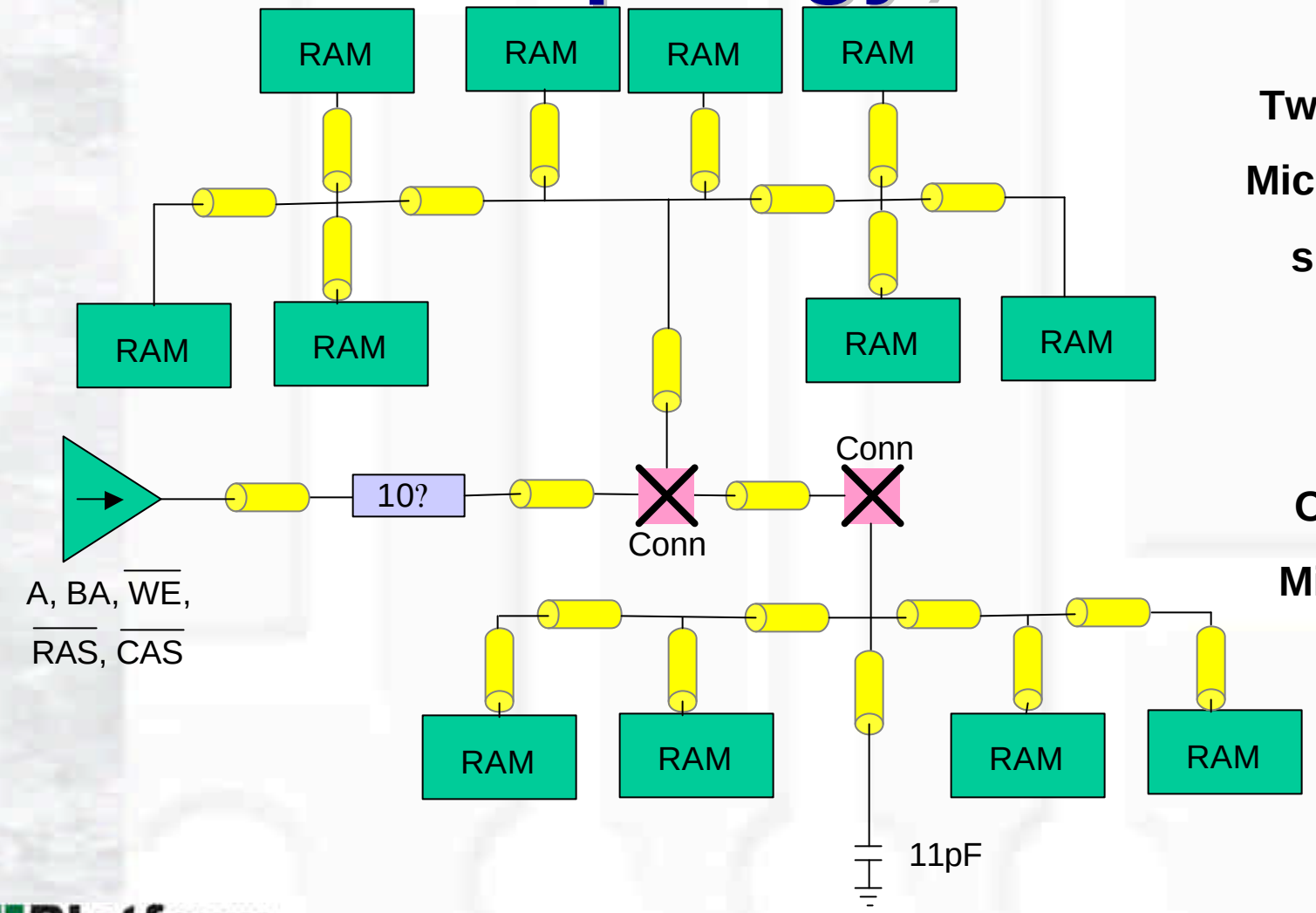
Two Bank MicroDIMM shown

A/C Topology, 1 Slot



One Bank MicroDIMM shown

A/C Topology, 2 Slot



Two Bank MicroDIMM shown

One Bank MicroDIMM shown

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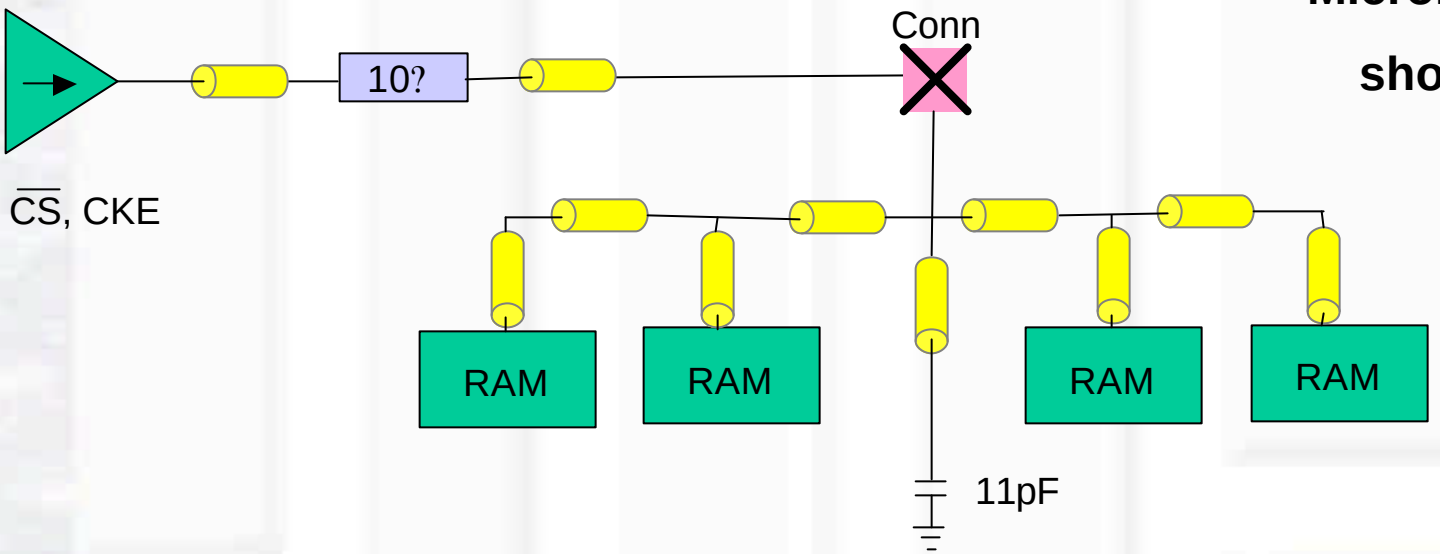
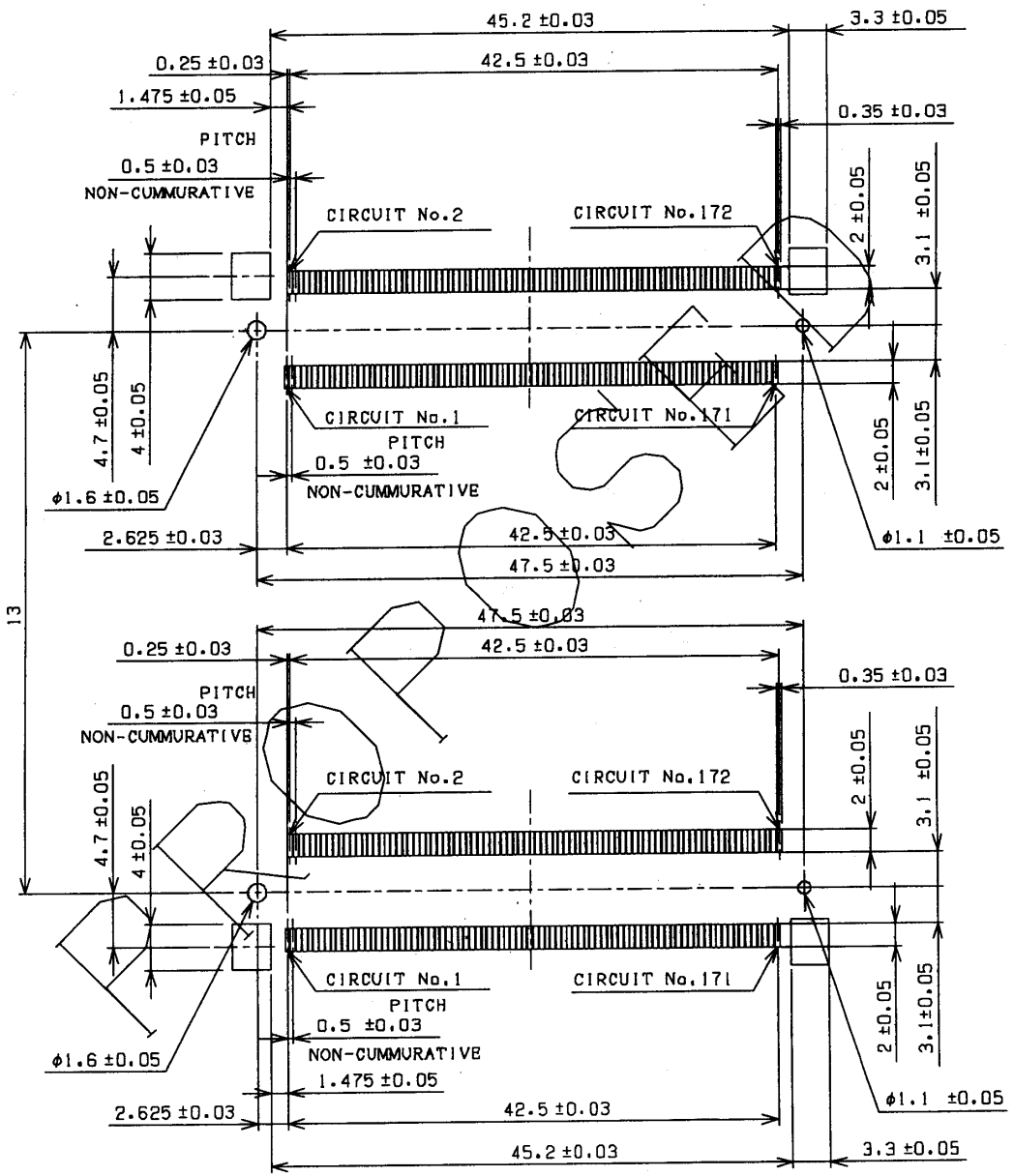
CS & CKE Topology

One or Two Bank MicroDIMM shown



Increasing Focus on Systems

- JEDEC packaging committee charter extended to include module sockets
  - Land pattern for pin pads
  - Mechanical support tab locations
  - Orientation holes
  - Shadow area of socket body
  - Module height & centerline
- Working system configuration first time!



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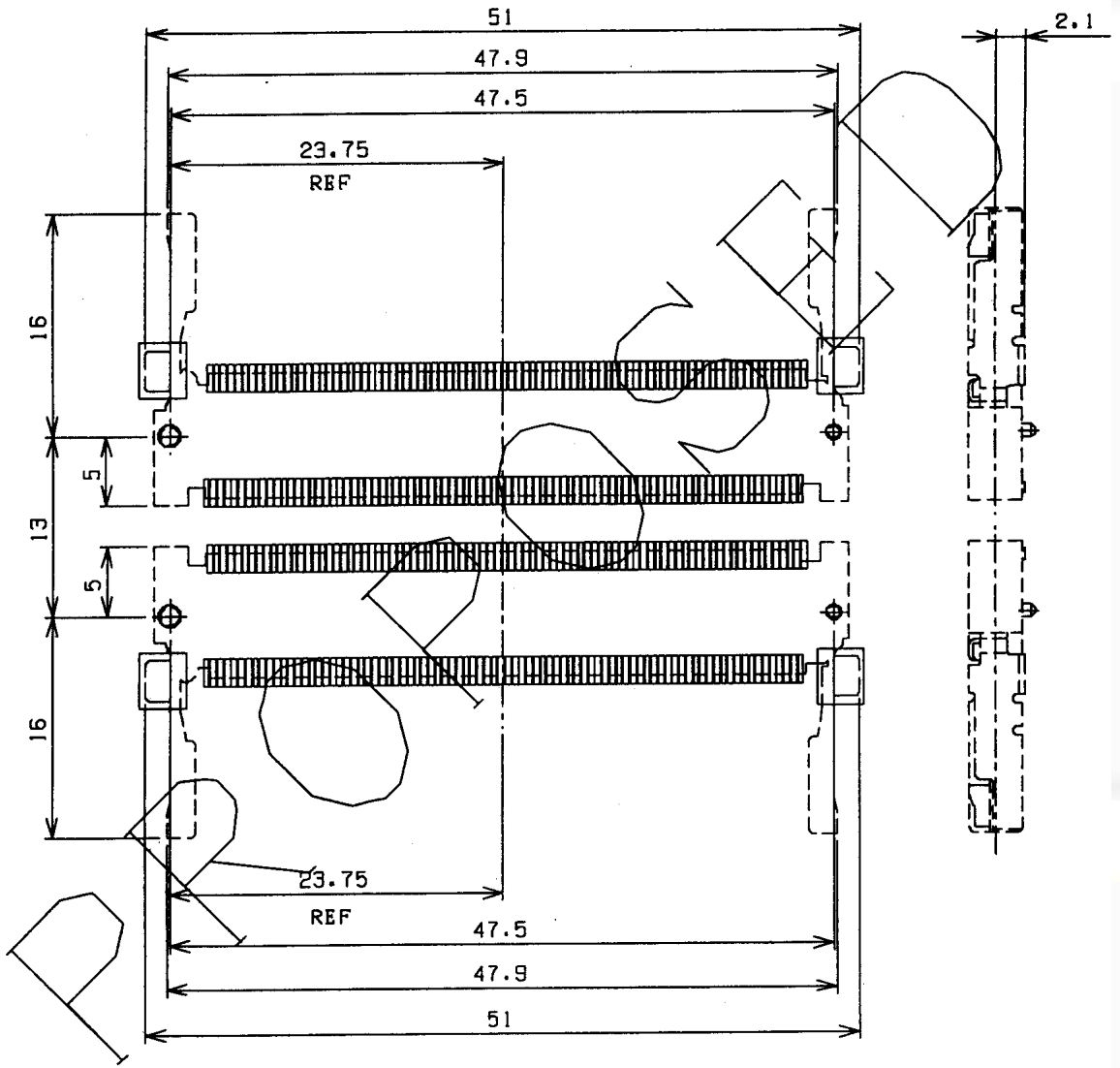
STANDARD TYPE



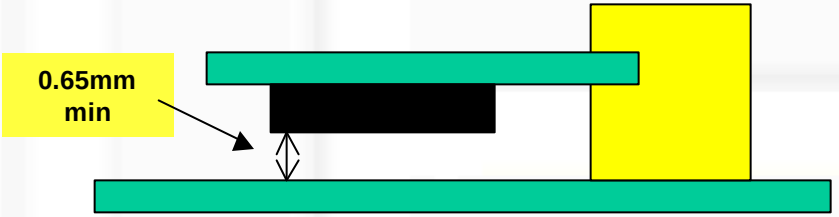
REVERSE TYPE

DDR MicroDIMM Clearances

Standard socket, double sided memory module

Standard socket, single sided memory module

Reverse socket, double sided memory module



Reverse socket, single sided memory module

Socket Spec Status

- Merging 144, 172 pin sockets into single parameterized MO-214 spec
  - Priming spring included
    - Shoves module “to the left”
  - Redimensioned by left edge, not center
  - Edge bezel defined

Conclusions

- DDR solutions for mobile growing
- Cached DRAM would be even better
- Point to point and DDR SO-DIMM done
- DDR333 development in progress
- FBGA packaged DDR coming
- DDR MicroDIMM development on track

Memory of choice for the future

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